AMENDMENTS TO THE SPECIFICATION:

Please amend the specification by inserting the following new section at page 1, line 15.

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of application serial no. 09/718,802, filed November 22, 2000, which application is incorporated herein in its entirety by this reference.

Please amend the paragraph on page 1, line 29 as follows:

Such non-volatile memory systems include an array of floating-gate memory cells and a system controller. The controller manages communication with the host system and operation of the memory cell array to store and retrieve user data. The memory cells are grouped together into blocks of cells, a block of cells being the smallest grouping of cells that are simultaneously erasable. Prior to writing data into one or more blocks of cells, those blocks of cells are erased. User data are typically transferred between the host and memory array in sectors. A sector of user data can be any amount that is convenient to handle, preferably less than the capacity of the memory block, often being equal to the standard disk drive sector size, 512 bytes. In one commercial architecture, the memory system block is sized to store one sector of user data plus overhead data, the overhead data including information such as an error correction code (ECC) for the user data stored in the block, a history of use of the block, defects and other physical information of the memory cell block. Various implementations of this type of non-volatile memory system are described in the following United States patents and pending applications assigned to SanDisk Corporation, each of which is incorporated herein in its entirety by this reference: Patents nos. 5,172,338, 5,602,987, 5,315,541, 5,200,959, 5,270,979, 5,428,621, 5,663,901, 5,532,962, 5,430,859 and 5,712,180, and application serial nos. 08/910,947, filed August 7, 1997, now patent no. 6,222,762, and 09/343,328, filed June 30, 1999, now patent no. 6,151,248.

Please amend the paragraph on page 2, line 11 as follows:

Another type of non-volatile memory system utilizes a larger size memory cell block that each stores multiple pages per block, a page being a minimum unit of data that is programmed as part of a single programming operation. One sector of user data, along with overhead data related to the user data and the block in which such data is being stored, are typically included in a page. Yet another specific system that has been commercially available from SanDisk Corporation for more than one year from the filing date hereof, stores overhead data related to the user data being stored, such as ECC, along with the user data in a common sector, while overhead data related to the block in which the sector is stored is written as part of a different sector in a different block. An example of this system is given in patent application serial no. 09/505,555, filed February 17, 2000, now patent no. 6,426,893, which ~~application~~ patent is incorporated herein in its entirety by this reference.

Please amend the paragraph on page 9, line 16 as follows:

A more recent variation used in a SanDisk product is illustrated in Figure 4. A primary difference with the data storage format of Figure 3 is that the block attributes are not stored in the same block as the user data. In a block 59, for example, 512 bytes of user data 61 are stored, and 8 bytes of ECC and flags are stored as user data attributes 63. This leaves a number of spare memory cells 65 in the block 59 that is sufficient to store 8 bytes of user and/or attribute data, to replace any defective cells within the block 59 in which user or attribute data would normally be stored. Attribute data 67 of the block 59 is stored in another block 69, and requires only 4 bytes. Indeed, the block 69 includes a number of such block attribute records for other blocks that contain user data. This data architecture is further described in aforementioned application serial no. 09/505,555, now patent no. 6,426,893.

Please amend the paragraph on page 12, line 12 as follows:

A different data structure of another block 121 is illustrated in Figure 9. Each page of that block, such as a page 123, stores a number of records of attribute (overhead) data that accompany the sectors of user data stored in other blocks such as the block ~~133~~ 103 of Figure 8. In one embodiment, the page 123 stores all, or nearly all, of the storage block attribute data for

the block ~~133~~ 103 and the user data attributes for each of the 33 user data sectors stored in that block. A specific example of the data structure for the page 123, and every other page written to the block 121, is shown in Figure 10. Since there are 32 pages in the block 121, there will be at least one attribute data block of the type of block 121 for every 32 user data blocks of the type of block 103.

Please amend the paragraph on page 12, line 29 as follows:

The attributes 125 (Figure 10) of the block 103 (Figure 8) are shown divided into physical and logical attributes, for purposes of discussion. The physical attributes, in this example, include a physical address (PBN) 135 of the user data block 103, and one or more other attributes 137 that can include an experience count of the number of times that the block has been erased, a programming voltage, an erase voltage, and the like. An ECC 139 may be provided for the fields 135 and 137. The logical attributes of the block 103 can include its logical address (LBN) 141 of the user data block 103, a time 143 at which the attribute page 123 was last written to the block 121, a transform flag 145 of the user data or the data within the page 123, and an ECC 147 of the fields 141, 143 and 145. The fields 131 and ~~135~~ 133 can be provided without an ECC.

Please amend the paragraph on page 15, line 22 as follows:

Application of the invention to another type of non-volatile memory system with a much different architecture is briefly described with respect to Figures 12 and 13. The memory array is divided into an even number of units, such as eight, two such units 0 and 1 being illustrated in Figure ~~2~~12. A pair of adjacent units, termed a plane, may share peripheral circuits, such as word line decoders. Each unit contains a large number of blocks of memory, such as a block 161 in the unit 0 and a block 163 in the unit 1. The individual blocks are in turn divided into multiple pages of memory.